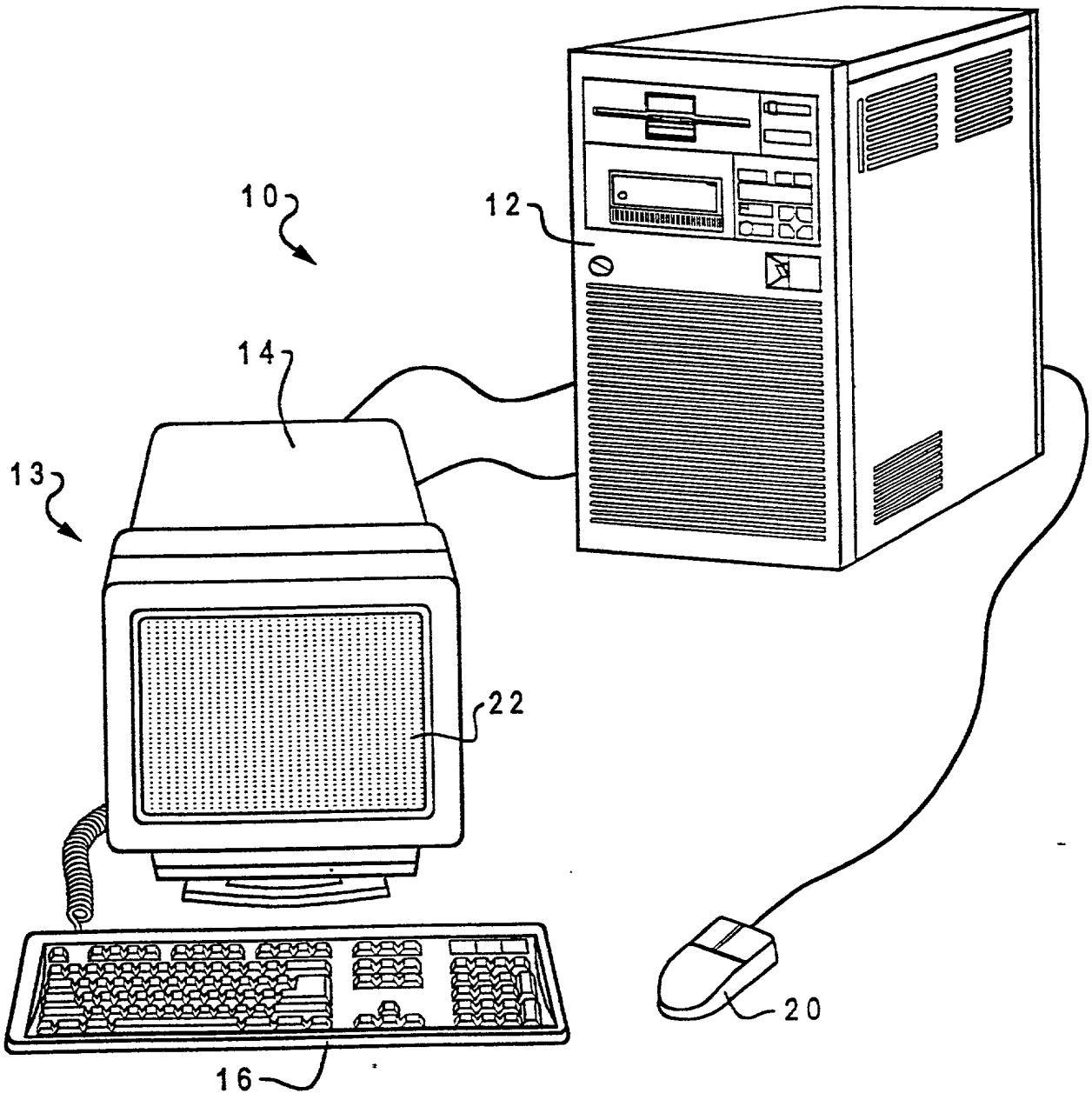

Fig. 1

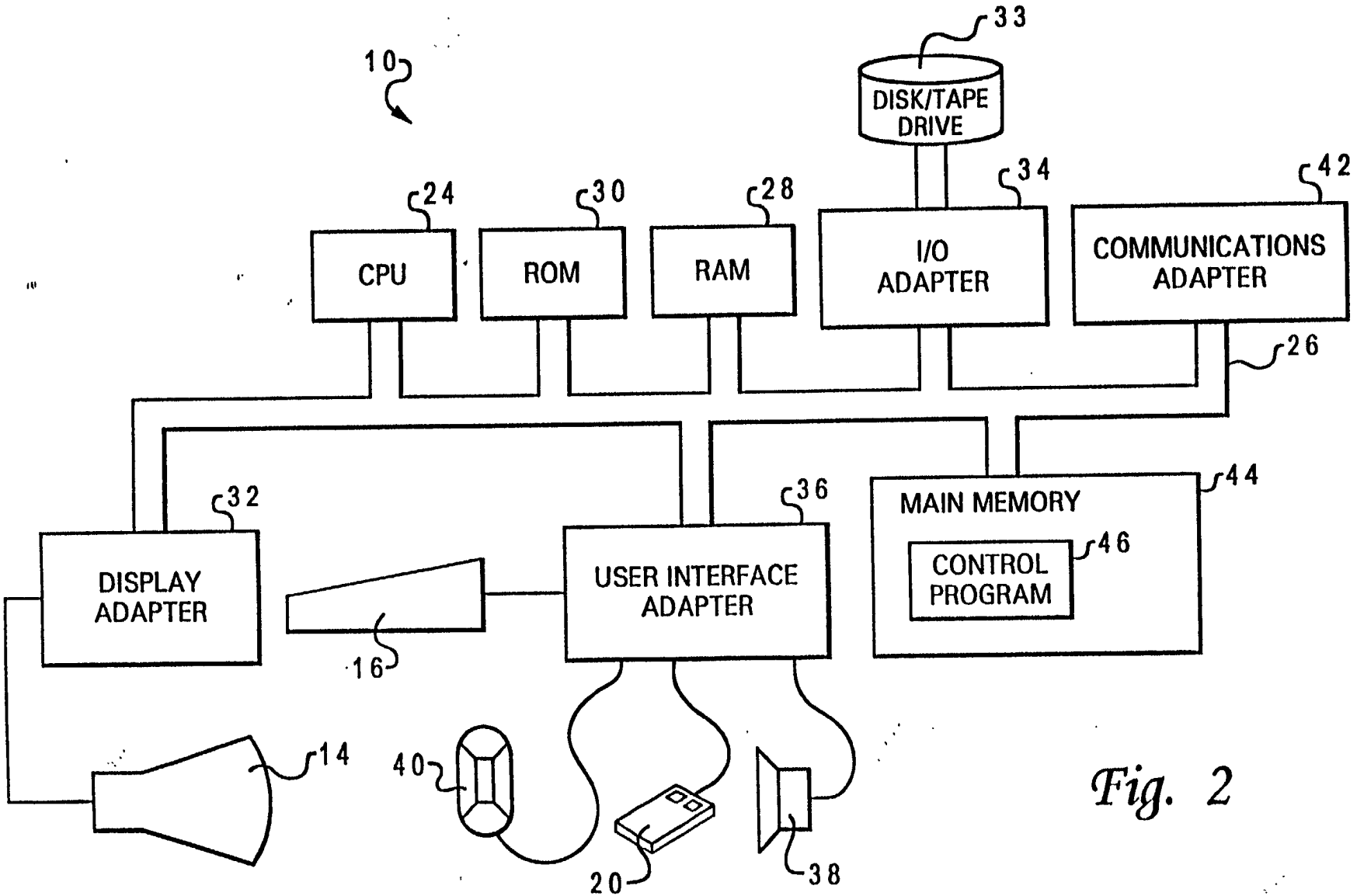

Fig. 2

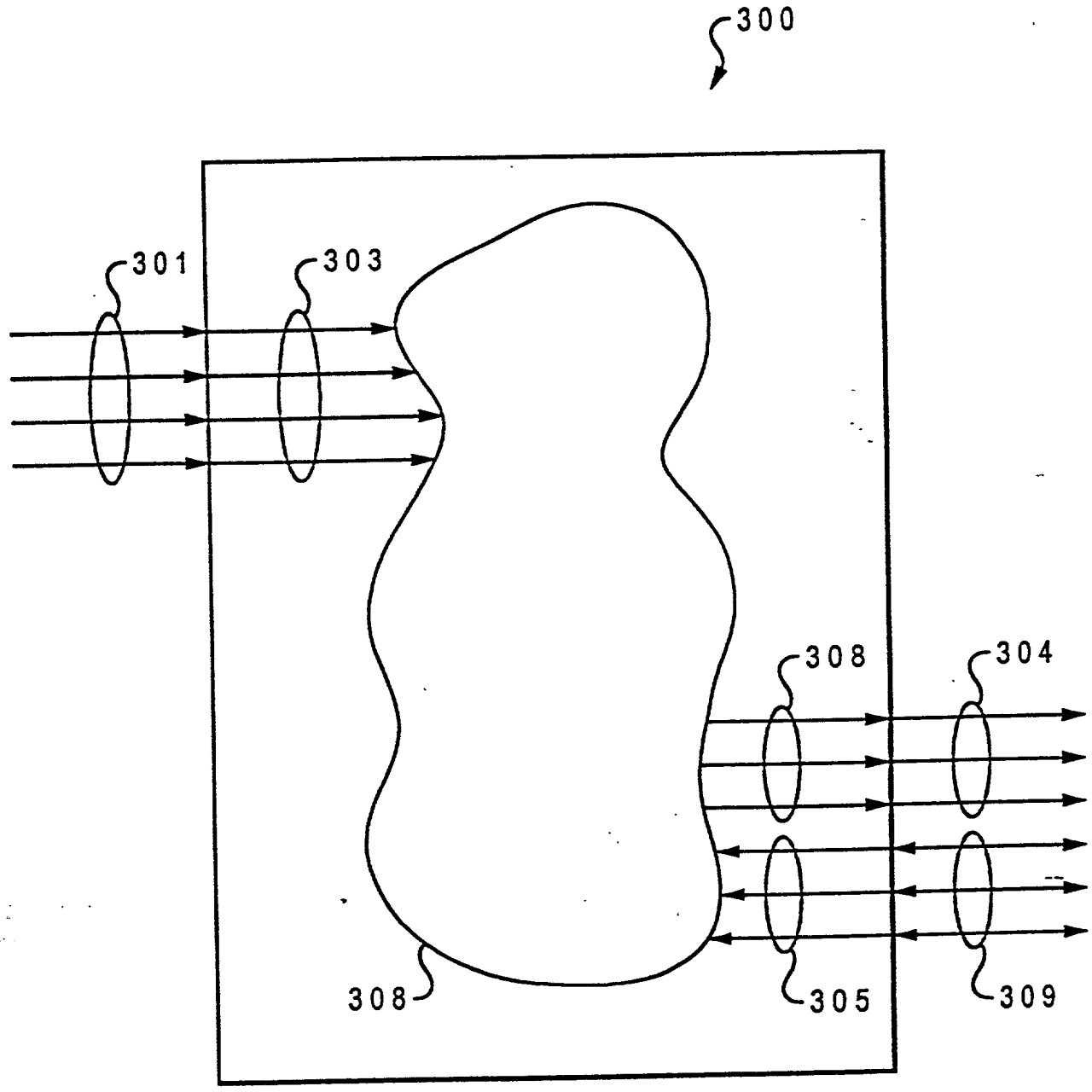

Fig. 3A

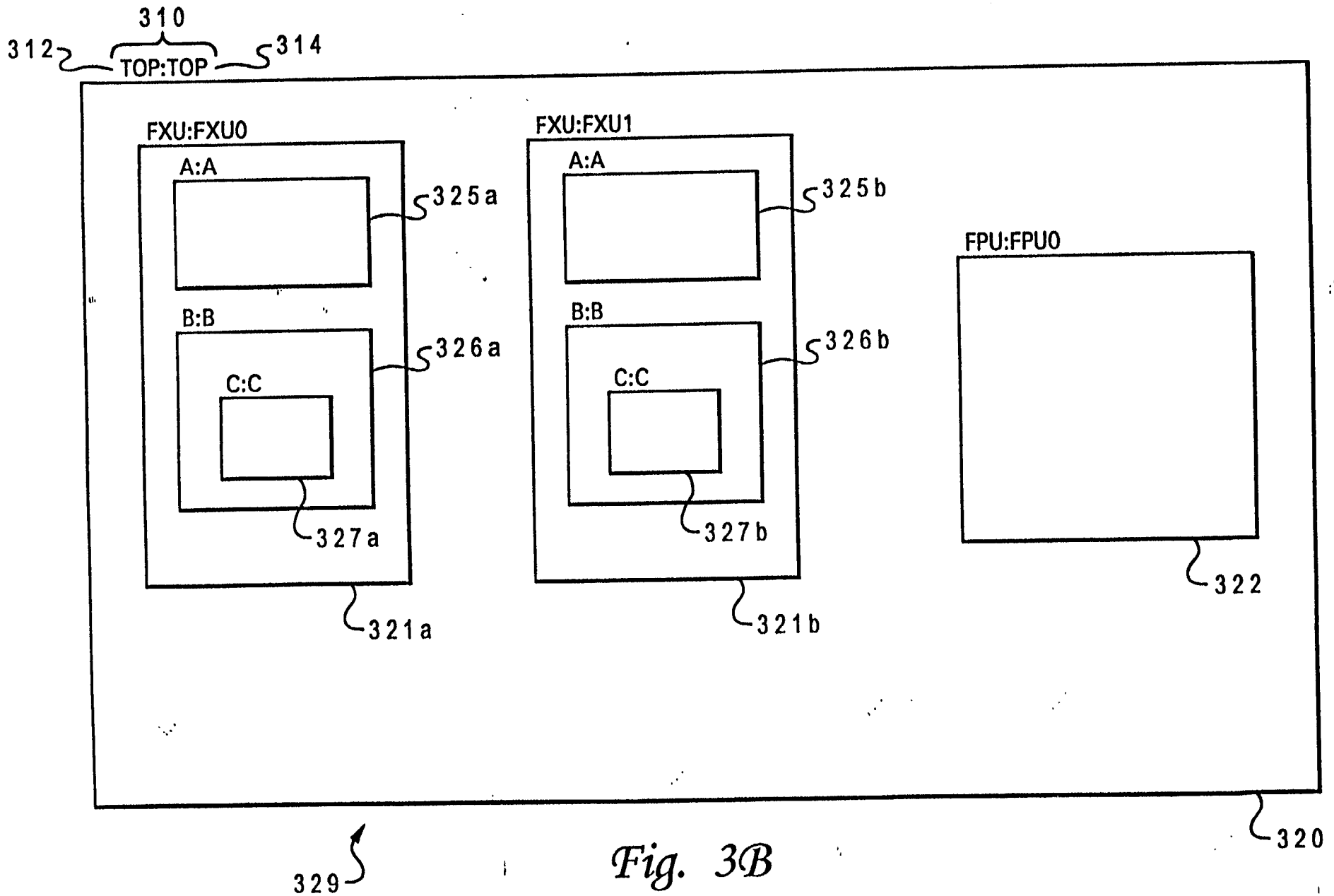
310
312
TOP:TOP
314
FXU:FXU0
A:A
325a
B:B
326a
C:C
327a
321a
FXU:FXU1
A:A
325b
B:B
326b
C:C
327b
321b
FPU:FPU0
322
320
329

Fig. 3B

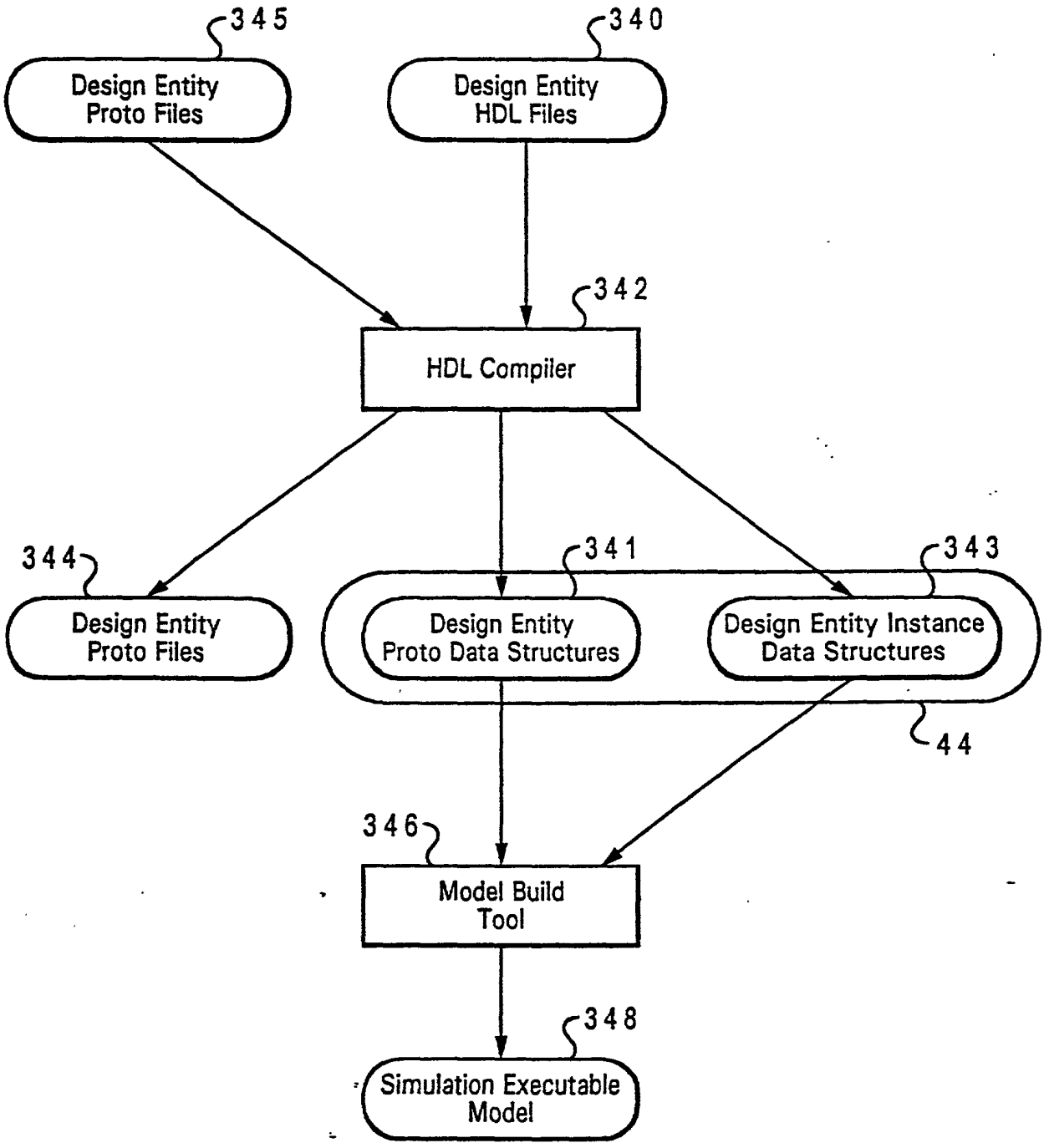
345
Design Entity
Proto Files
340
Design Entity
HDL Files
342
HDL Compiler
344
Design Entity
Proto Files
341
Design Entity
Proto Data Structures
343
Design Entity Instance
Data Structures
44
346
Model Build
Tool
348
Simulation Executable
Model

Fig. 3C

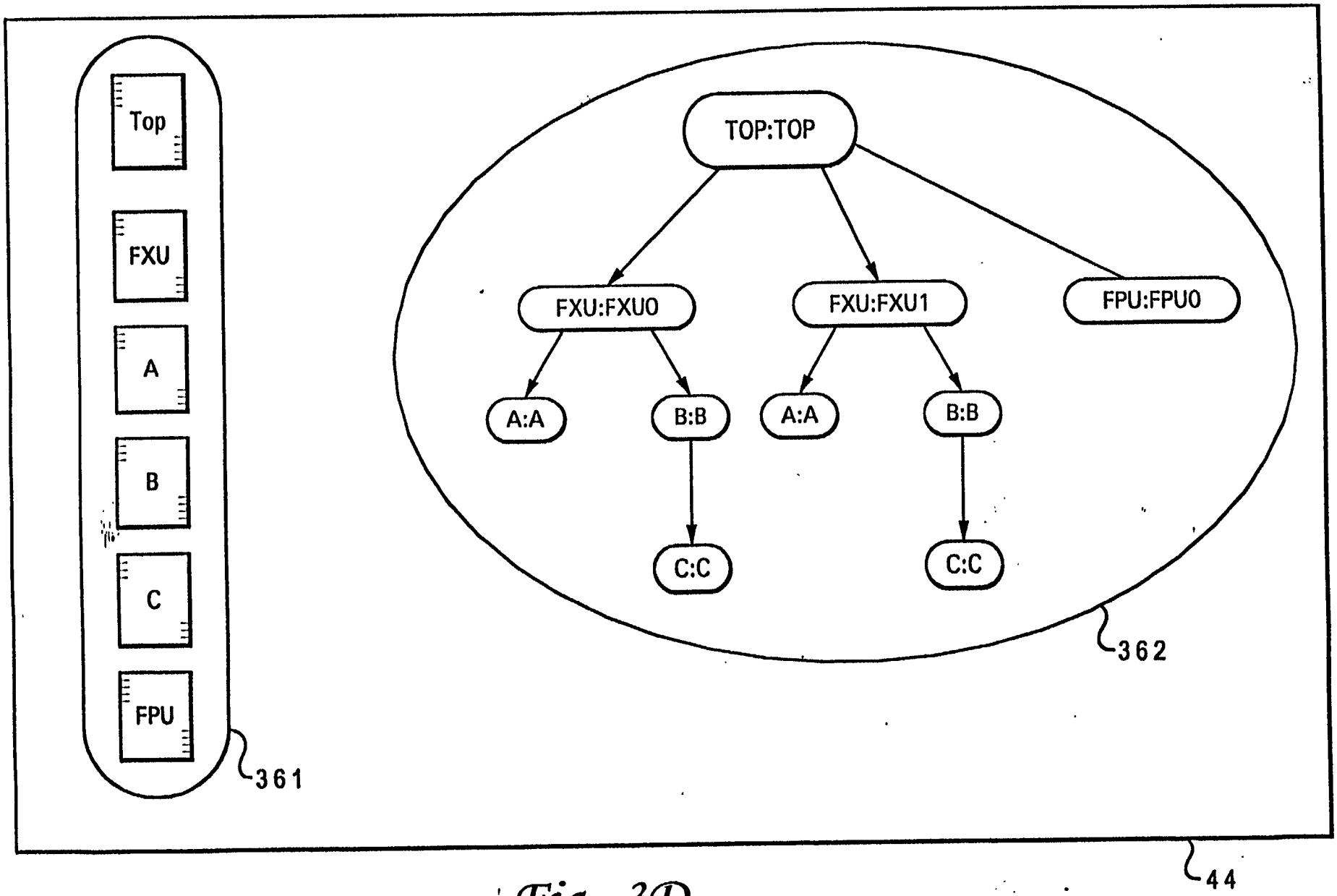
Top
FXU
A
B
C
FPU
361
TOP:TOP
FXU:FXU0
FXU:FXU1
FPU:FPU0
A:A
B:B
A:A
B:B
C:C
C:C
362
44

Fig. 3D

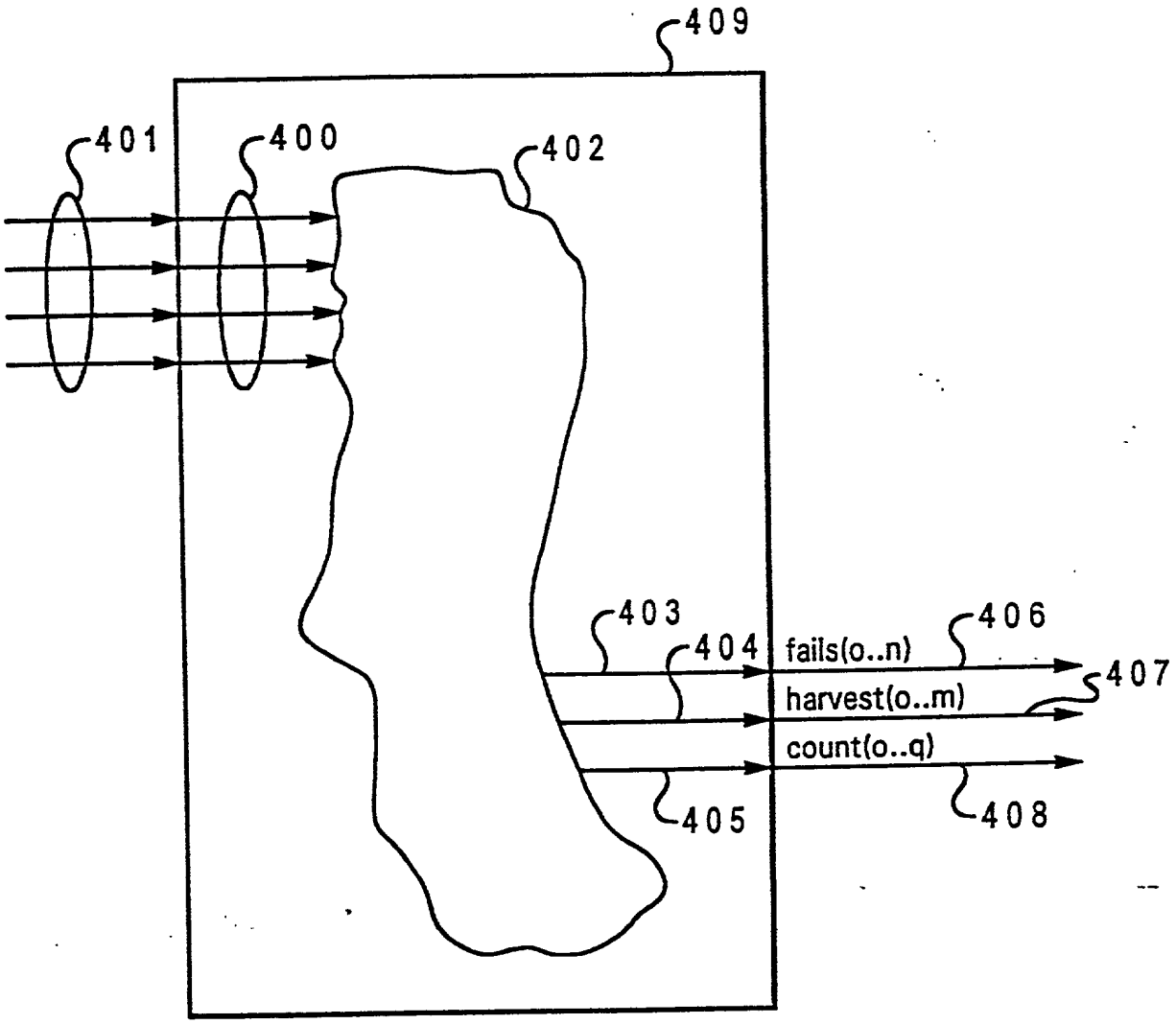
409
401
400
402
403
404
406
fails(o..n)
407
harvest(o..m)
count(o..q)
405
408

Fig. 4A

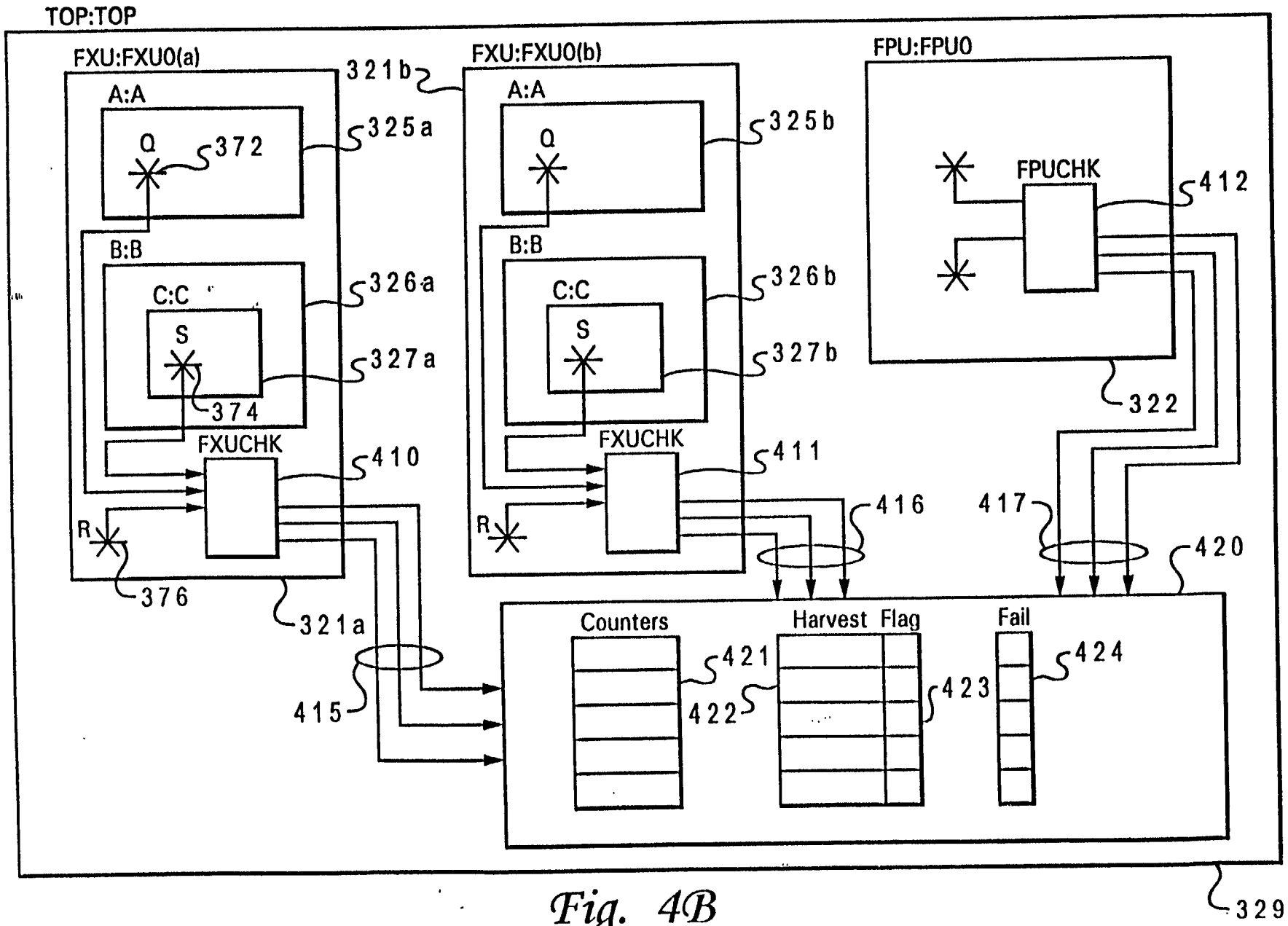
TOP:TOP
FXU:FXU0(a)
A:A
Q
372
325a
B:B
C:C
S
374
326a
327a
FXUCHK
410
R
376
321a
321b
FXU:FXU0(b)
A:A
Q
325b
B:B
C:C
S
326b
327b
FXUCHK
411
R
416
FPU:FPU0
FPUCHK
412
322
417
420
Counters
421
422
Harvest Flag
423
Fail
424
415
329

Fig. 4B

```
ENTITY FXUCHK IS

    PORT(   S_IN        :    IN std_ulogic:
            Q_IN        :    IN std_ulogic:
            R_IN        :    IN std_ulogic:
            clock       :    IN std_ulogic:
            fails       :    OUT std_ulogic_vector(0 to 1);
            counts      :    OUT std_ulogic_vector(0 to 2);
            harvests    :    OUT std_ulogic_vector(0 to 1);
        );

--!! BEGIN
--!! Design Entity: FXU;

--!! Inputs
--!! S_IN        =>    B.C.S;
--!! Q_IN        =>    A.Q;
--!! R_IN        =>    R;
--!! CLOCK       =>    clock;
--!! End Inputs

--!! Fail Outputs;
--!! 0 : "Fail message for failure event 0";
--!! 1 : "Fail message for failure event 1";
--!! End Fail Outputs;

--!! Count Outputs;
--!! 0 : <event0> clock;
--!! 1 : <event1> clock;
--!! 2 : <event2> clock;
--!! End Count Outputs;

--!! Harvest Outputs;
--!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;

--!! End;

ARCHITECTURE example of FXUCHK IS

BEGIN

    ... HDL code for entity body section ...

END;
```

450 452 453 454 455 456 457 451 458 440

Fig. 4C

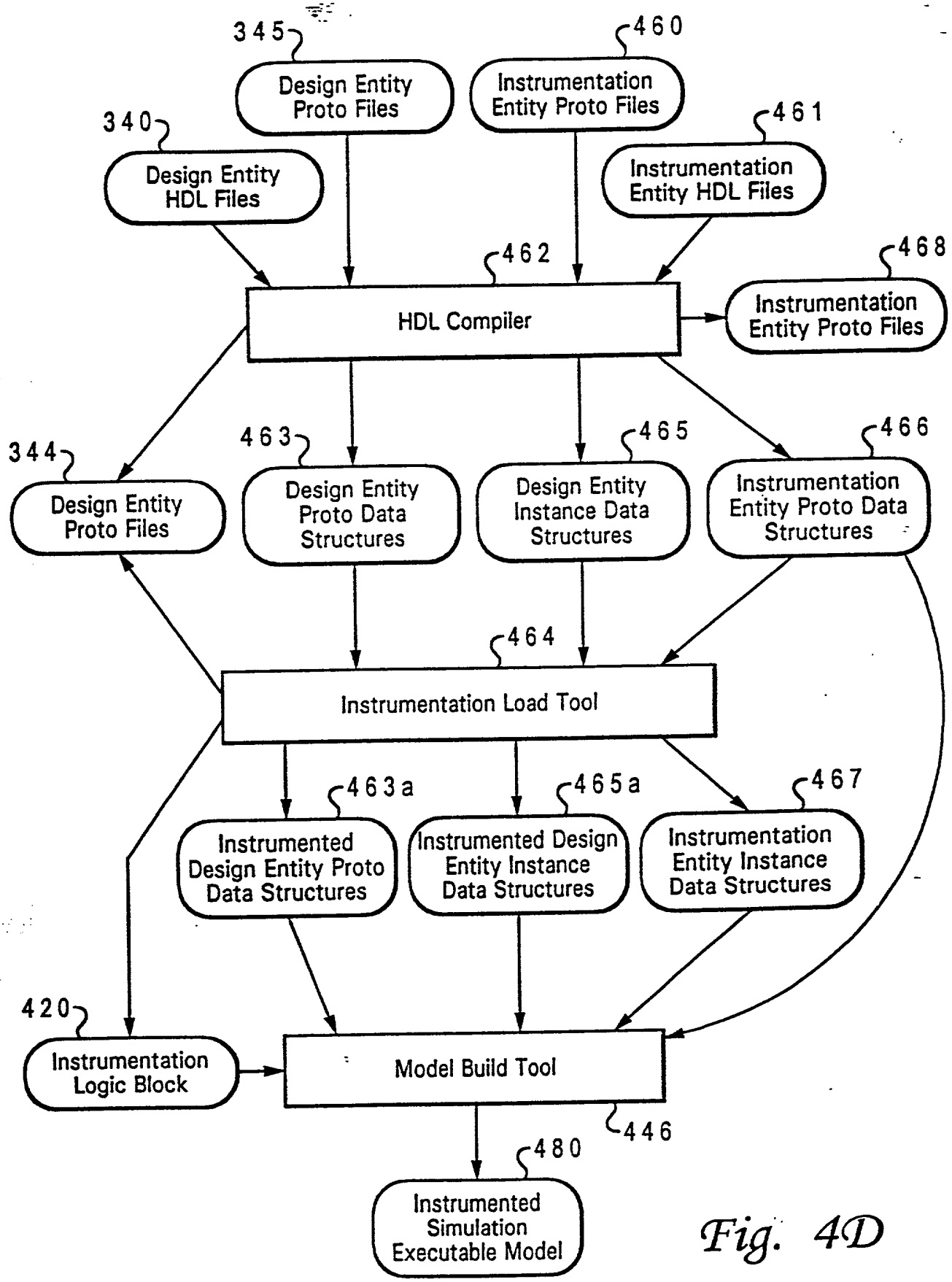
345
Design Entity Proto Files
460
Instrumentation Entity Proto Files
340
Design Entity HDL Files
461
Instrumentation Entity HDL Files
462
HDL Compiler
468
Instrumentation Entity Proto Files
344
Design Entity Proto Files
463
Design Entity Proto Data Structures
465
Design Entity Instance Data Structures
466
Instrumentation Entity Proto Data Structures
464
Instrumentation Load Tool
463a
Instrumented Design Entity Proto Data Structures
465a
Instrumented Design Entity Instance Data Structures
467
Instrumentation Entity Instance Data Structures
420
Instrumentation Logic Block
Model Build Tool
446
480
Instrumented Simulation Executable Model

Fig. 4D

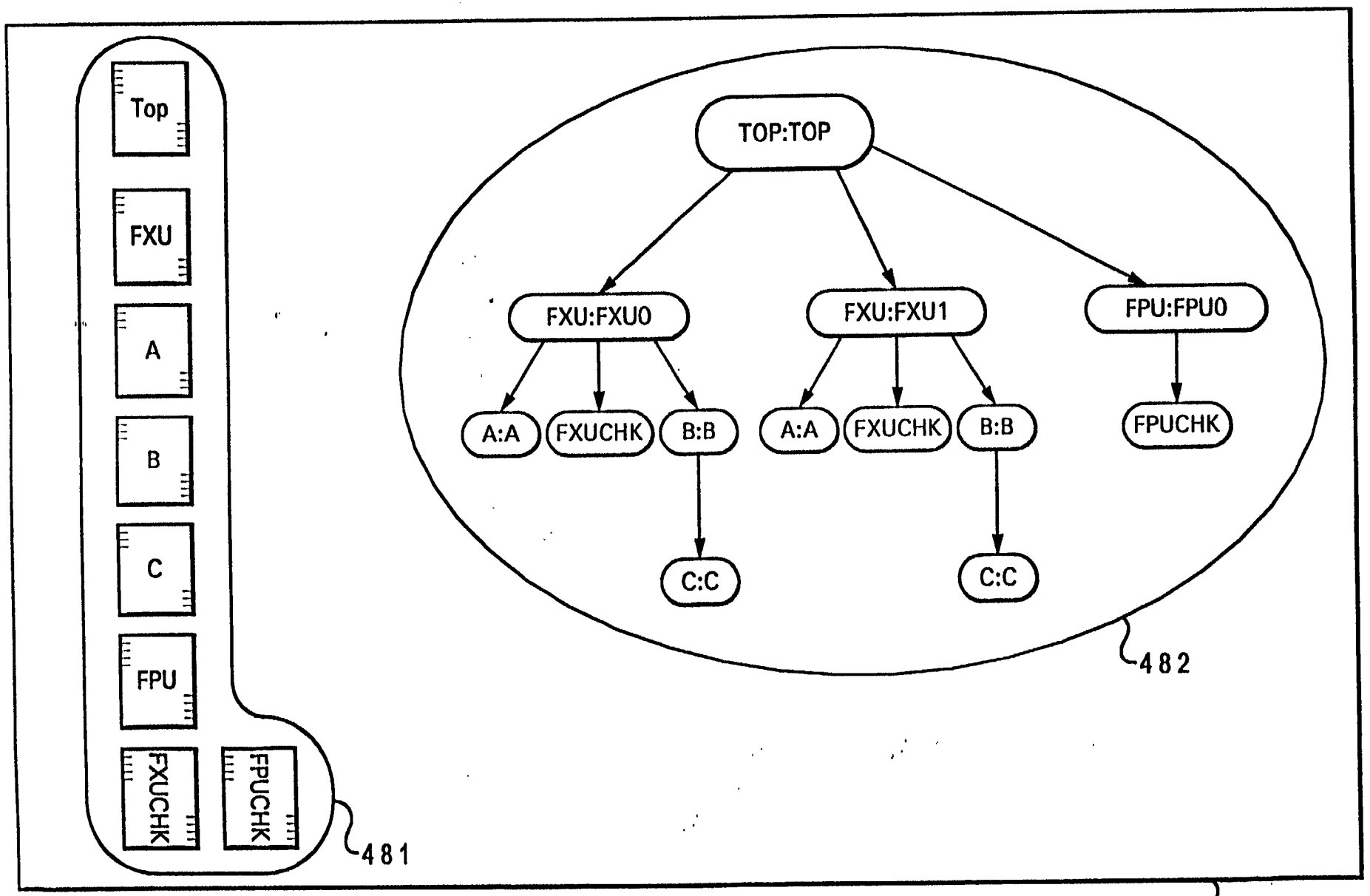
Top
FXU
A
B
C
FPU
FXUCHK
FPUCHK
481
TOP:TOP
FXU:FXU0
FXU:FXU1
FPU:FPU0
A:A
FXUCHK
B:B
A:A
FXUCHK
B:B
FPUCHK
C:C
C:C
482
44

Fig. 4E

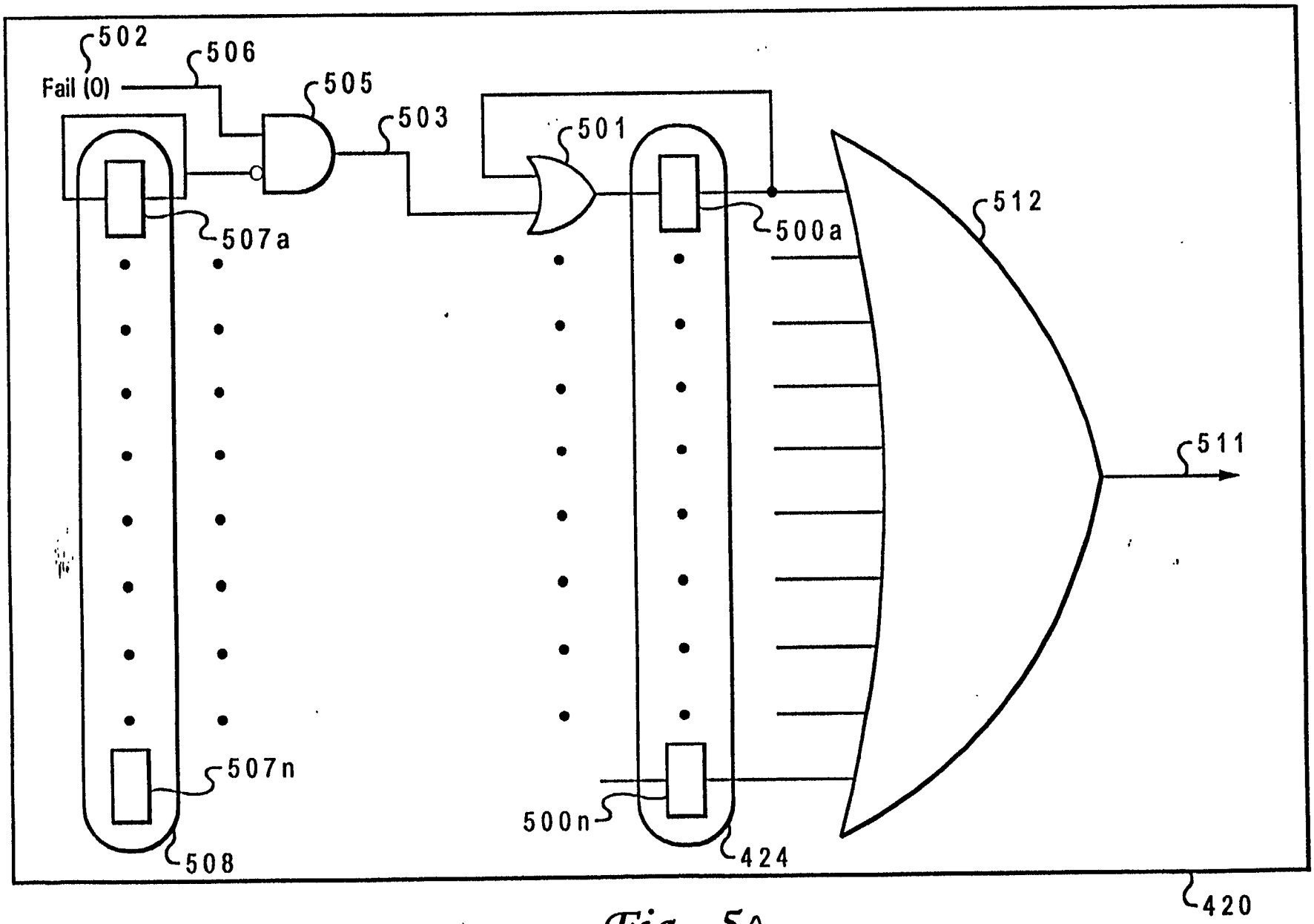
502
Fail (0)
506
505
503
501
507a
500a
512
511
507n
500n
508
424
420

Fig. 5A

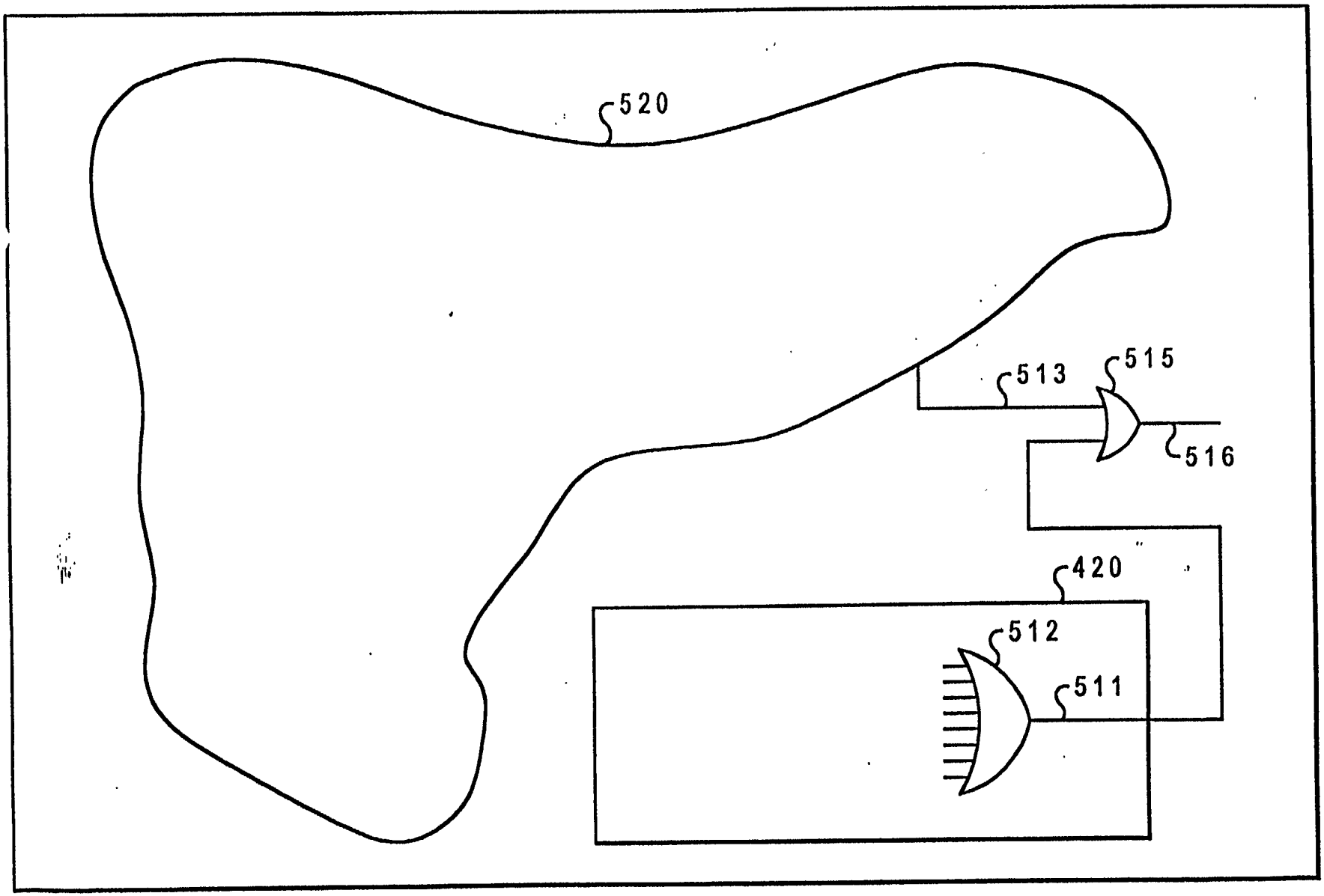

Fig. 5B

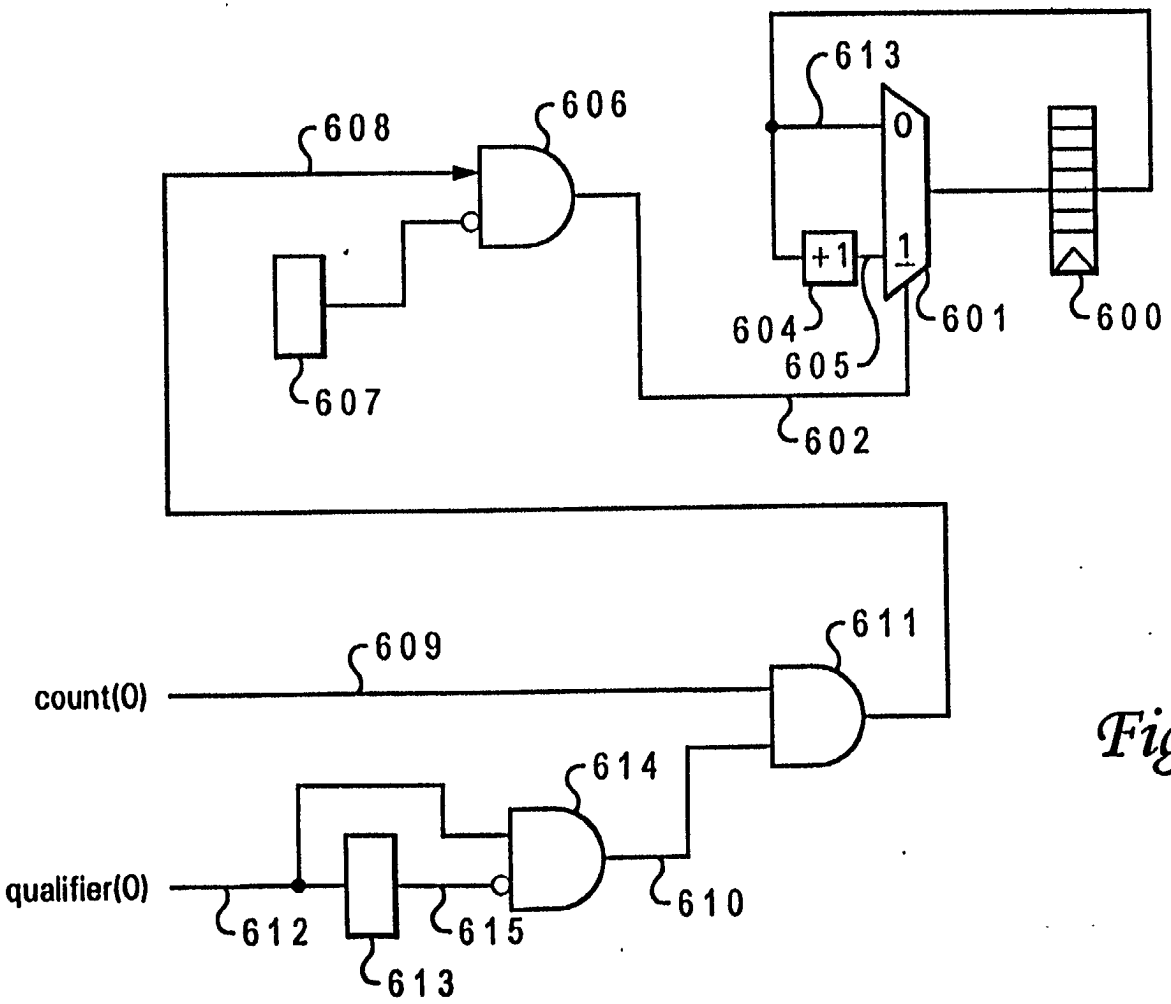
613
606
608
0
1
+1
604
605
601
600
607
602
611
609
count(0)
614
qualifier(0)
612
615
610
613

Fig. 6A

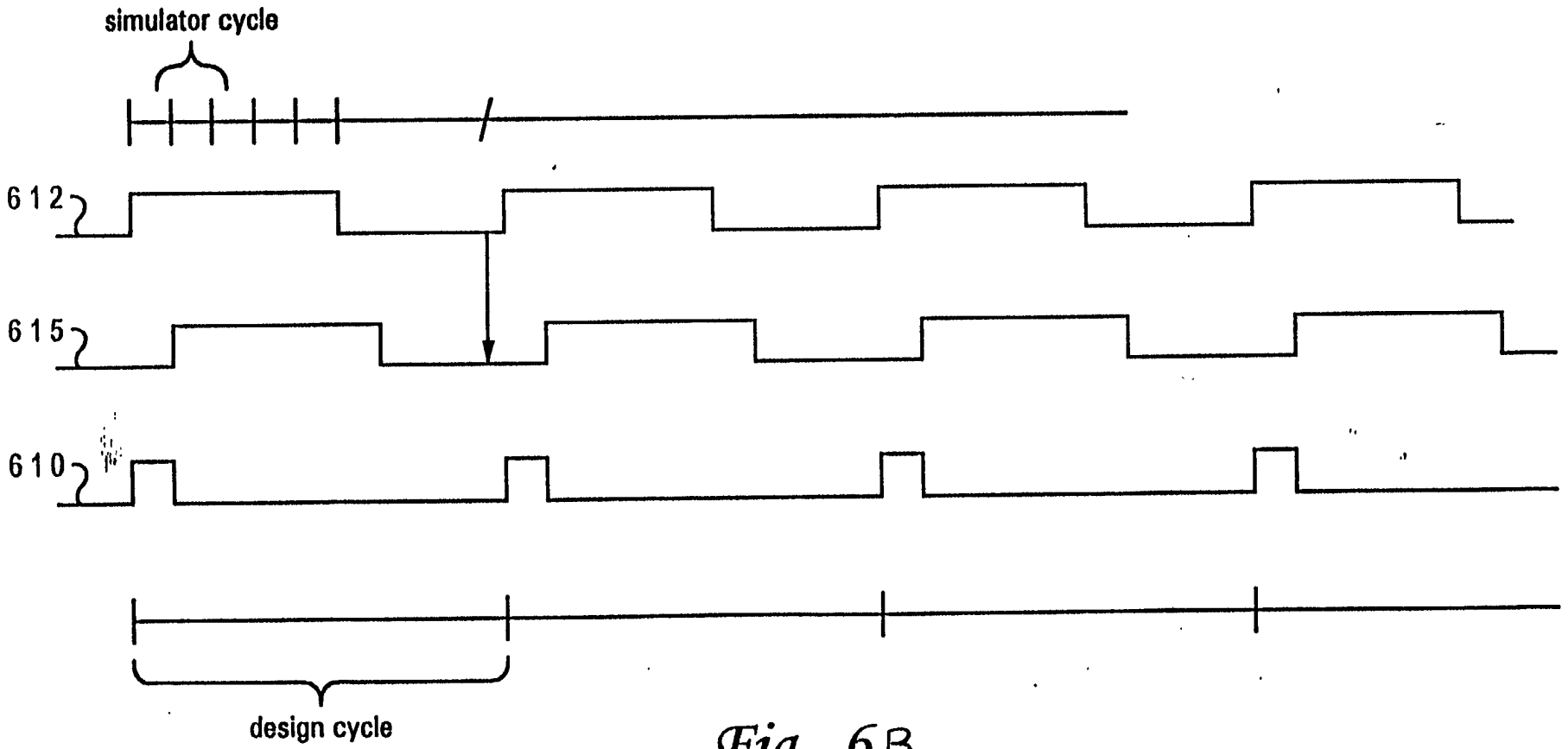

Fig. 6B

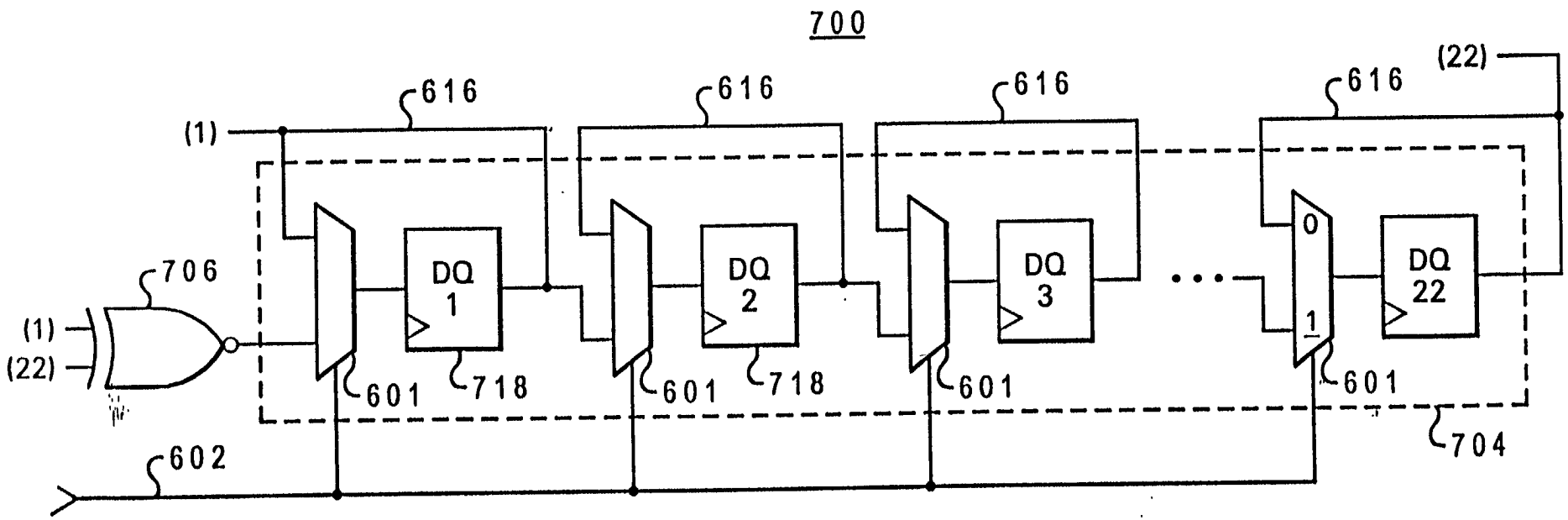

Fig. 7

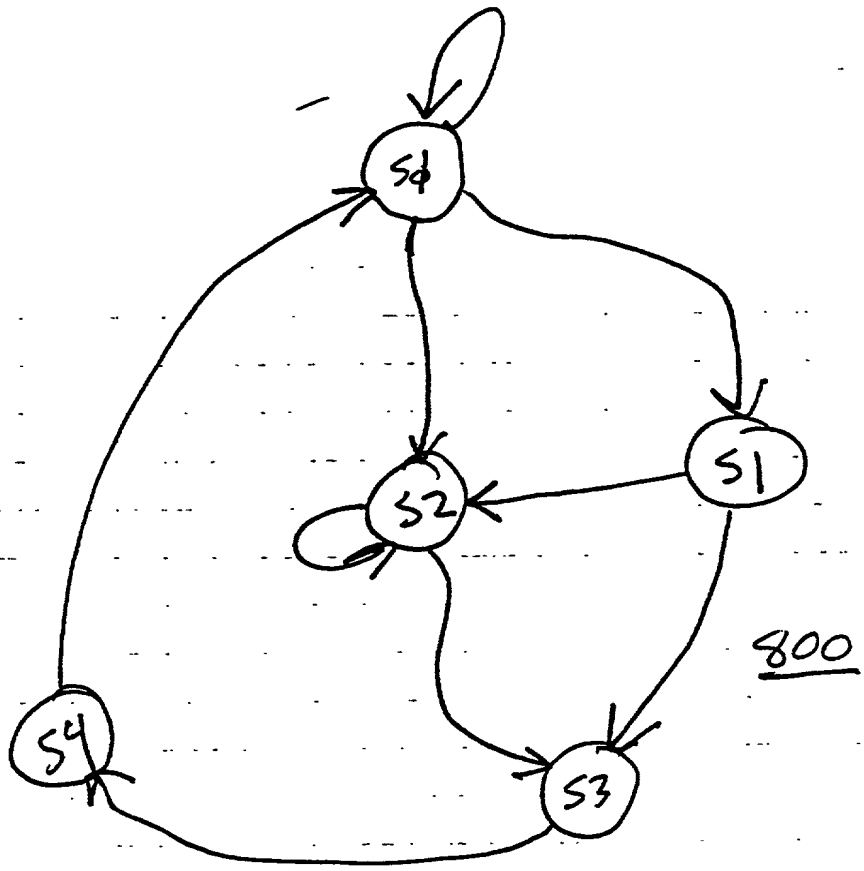

FIG. 8

(Prior Art)

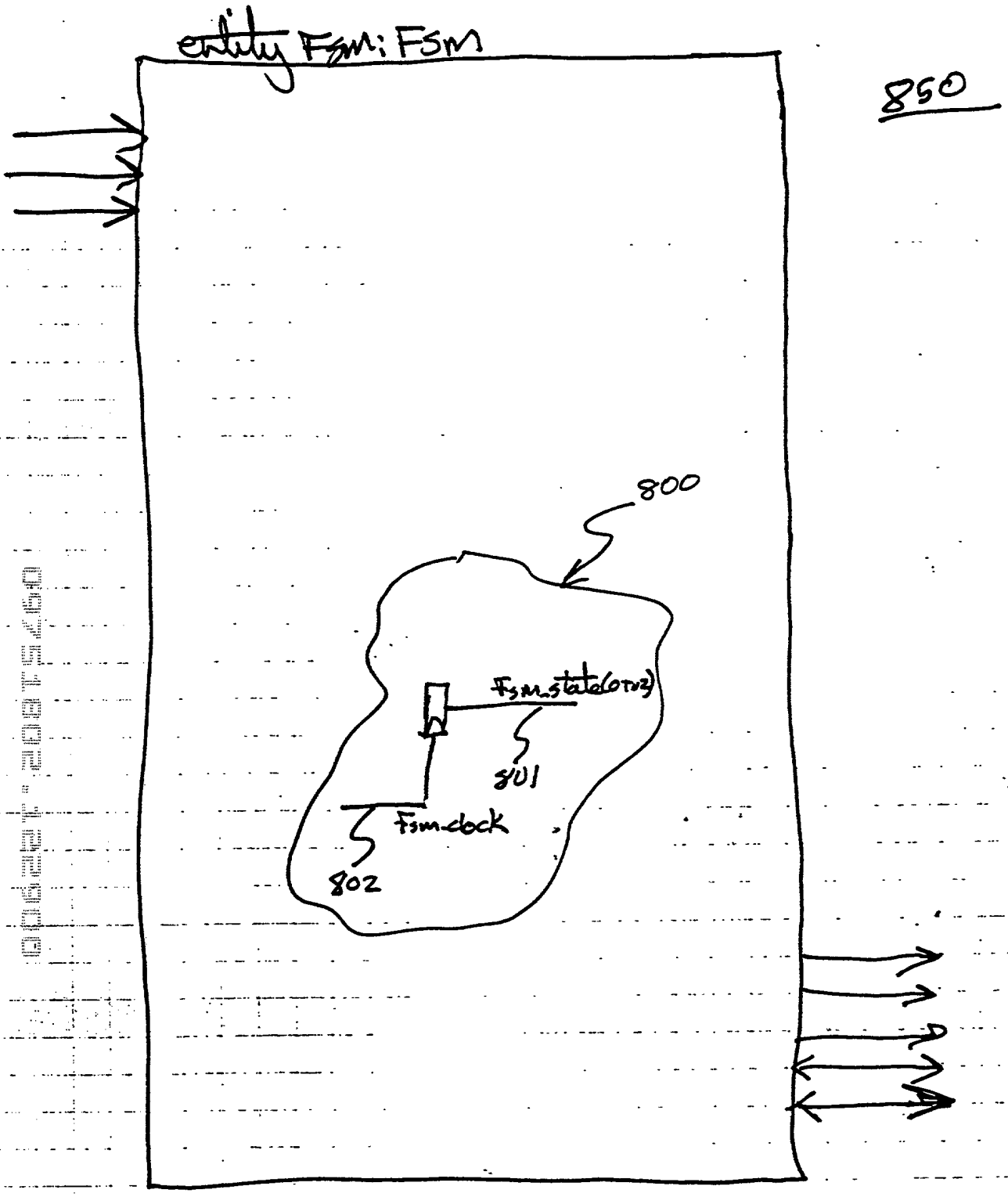

FIG. 8A
(Prior Art)

```
entity Fsm IS
  PORT(
        .... ports for entity Fsm .....
  );
ARCHITECTURE Fsm of Fsm IS
BEGIN
        .... HDL code For Fsm and rest of the entity...

        fsm_state(0 to 2) <= ... signal 801 ....

853 {   --!! Embedded Fsm : exampleFsm;
859 {   --!! clock        : (fsm_clock);
854 {   --!! state_vector : (fsm_state(0 to 2));
855 {   --!! states       : (s0,s1,s2,s3,s4);
856 {   --!! state_encoding : ('000', '001', '010', '011', '100');
857 [   --!! arcs         : (s0=>s0, s0=>s1, s0=>s2,
        --!!                s1=>s2, s1=>s3, s2=>s2,
        --!!                s2=>s3, s3=>s4, s4=>s0);
858 {   --!! end Fsm;

END;
```

852

85

FIG. 8B

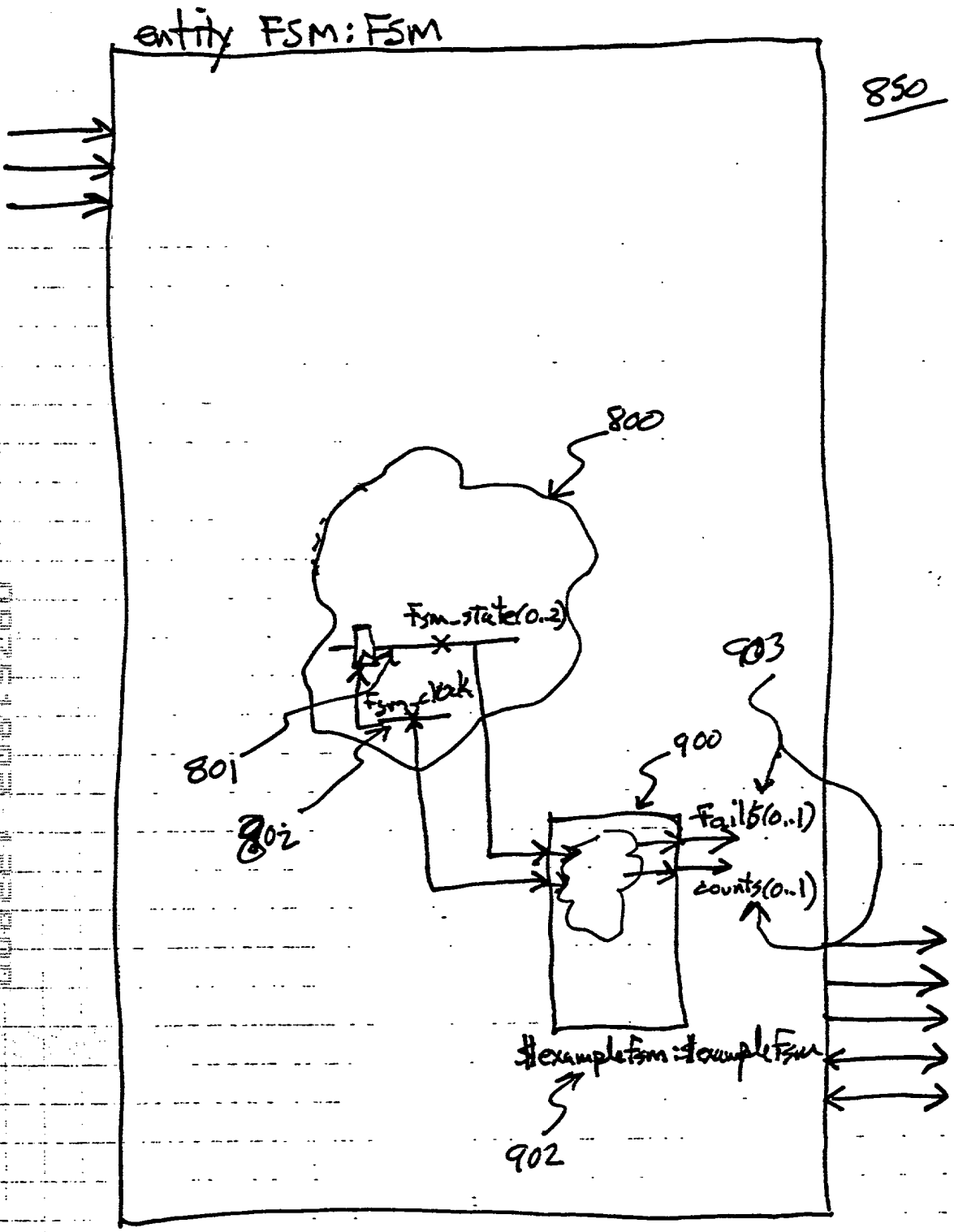
entity FSM:FSM
850
800
fsm_state(0..2)
fsm_clock
801
802
903
900
Failb(0..1)
counts(0..1)
$exampleFsm:exampleFsm
902

FIG. 9

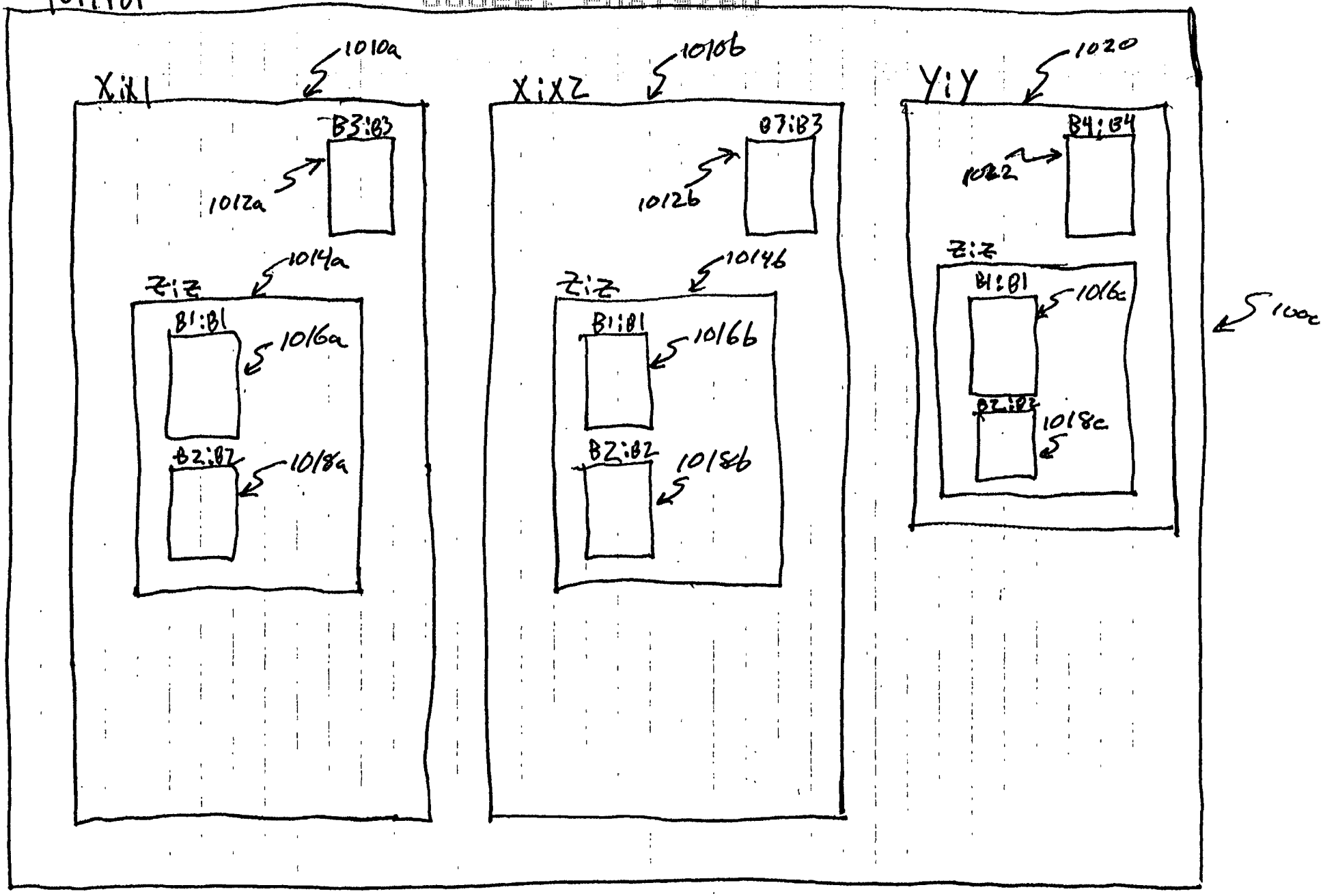
TOP:TOP
X:X1
1010a
B3:B3
1012a
Z:Z
1014a
B1:B1
1016a
B2:B2
1018a
X:X2
1010b
B3:B3
1012b
Z:Z
1014b
B1:B1
1016b
B2:B2
1018b
Y:Y
1020
B4:B4
1022
Z:Z
B1:B1
1016c
B2:B2
1018c
100c

FIG. 10A

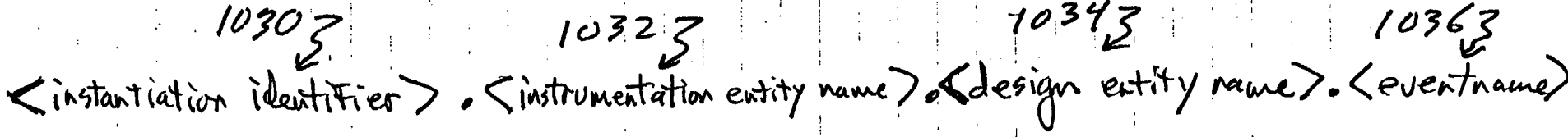

FIG 10B

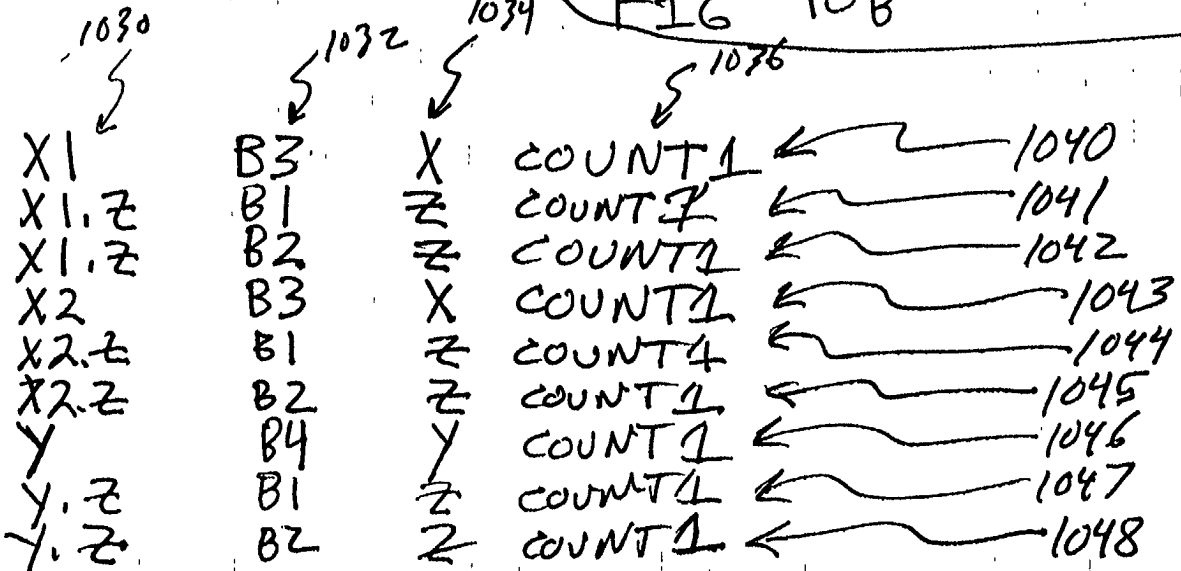

FIG 10C

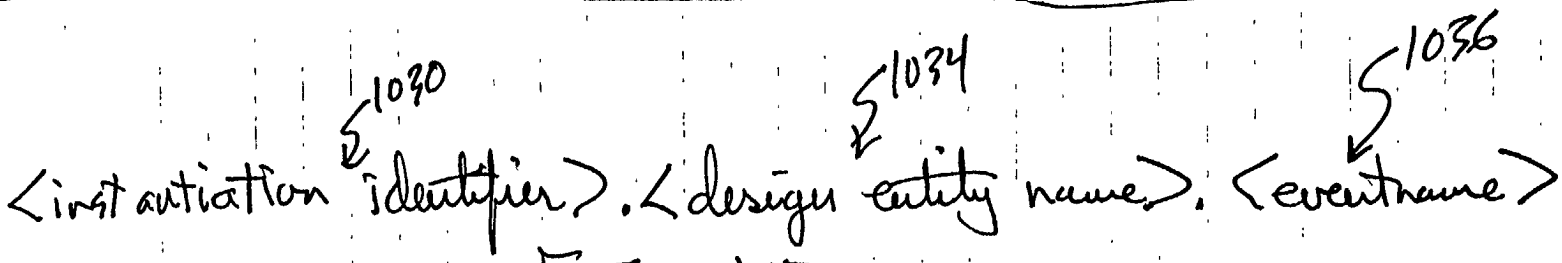

FIG. 10D